Ultra-Low Phase Noise Frequency Division With Array of Direct Digital Synthesizers

Marco Pomponio, Archita Hati, *Member, IEEE*, and Craig Nelson, *Member, IEEE*

***Abstract*— In this article, we present a four-channel direct digital synthesis (DDS) design that operates with a common clock ranging from 500 MHz to 24 GHz and generates output frequencies up to 1.75 GHz. A key feature of this board is its custom field-programmable gate array (FPGA)-based synchronization method, which ensures alignment accuracy of 170 ps between the channels, enabling precise frequency and phase relationship settings. In addition, the DDS board incorporates a user-friendly web interface that allows for continuous control and monitoring capabilities over TCP/IP. Multiple synchronized channels can be power-combined to produce a low-phase noise output due to coherent addition of the common carriers and the noncoherent addition of the residual DDS noise. By exploiting these principles and combining eight parallel channels of two DDS boards, we achieve exceptional residual phase noise performance, with $\mathscr{L}(1\text{ Hz}) = -147$ dBc/Hz and $\mathscr{L}(100\text{ kHz}) = -180$ dBc/Hz for a 9.765625 MHz output signal. These noise levels surpass the previously reported results achieved with regenerative frequency dividers. We also present a method for obtaining accurate residual noise measurements using an absolute phase modulation (PM) noise and amplitude modulation (AM) noise analyzer. Furthermore, we analyze the phase alignment tolerances required to minimize the AM-to-PM and PM-to-AM conversion that commonly occurs in power-combined signals. Finally, we demonstrate the synthesis of a highly stable 9.765625 MHz signal obtained from a cavity-stabilized optical frequency comb (OFC), with an absolute white phase noise of −180 dBc/Hz.**

***Index Terms*— Amplitude modulation (AM) noise, direct digital synthesis (DSS), field-programmable gate array (FPGA), frequency division, phase modulation (PM) noise, time-to-digital converter (TDC).**

I. Introduction

LOW-NOISE frequency synthesis, which is the generation of new and different carrier frequencies from a set of existing fixed frequency sources or clocks, is a critical component of many applications such as telecommunication systems [1], [2], phase-locked loops (PLLs) [3], optical frequency tracking [4], optical transfer oscillators [5], and radar [6], [7], [8]. The three most important operations in frequency synthesis are frequency multiplication, division, and translation, which must be implemented in a low-noise fashion to not degrade the newly synthesized signals. Direct digital synthesis (DDS), which can act as a source and a programmable frequency divider, has gained widespread adoption in frequency synthesis, due to advancements in field-programmable gate array (FPGA) technology and the availability of compact, high-performance single-chip implementations. DDS offers fast and precise control of a signal's frequency, amplitude, and phase, making it an ideal choice for frequency synthesis. Although DDS may not match analog electronics in terms of phase modulation (PM) and amplitude modulation (AM) noise [9], and spurious responses due to phase truncation [10], [11], its convenience and phase continuity with frequency changes make it an invaluable resource.

The state-of-the-art low-phase noise frequency division can be accomplished using regenerative dividers [12], [13], which can produce exceptional residual phase noise. However, these circuits need to be designed and tuned for a specific frequency and division factor. Frequency division with PLLs [14] offers some flexibility in division or multiplication factors and can exhibit good residual phase noise within the PLL bandwidth, while outside it is mostly dominated by the phase noise of the voltage-controlled oscillator (VCO). Improving residual phase noise in a PLL circuit is not trivial, since the main limitation is determined by the phase detector's residual noise. Summing multiple PLL outputs to reduce the residual phase noise is also difficult to achieve since fine control of their relative phase is needed to avoid AM-to-PM conversion, as this article will demonstrate. If external phase shifters are used, it will make the overall circuit bulky and difficult to tune. In contrast, in a DDS-based frequency division, the output/input frequency ratios are highly flexible, and the residual phase noise relies solely on numerical quantization and the quality of the digital-to-analog converter (DAC). In this last case, power summing DDS outputs to further reduce their residual phase noise is, on the other hand, easier than other types of frequency division circuits due to the flexibility of their digital implementation. In fact, finely tuning the different outputs' relative phase and amplitude is achieved with simple commands, allowing for almost perfect summation without AM-to-PM noise conversion.

In this article, we present the design and noise performance of a four-channel DDS synthesizer board connected to a common input frequency reference. The DDS outputs can be used independently or summed with external power combiners to improve the overall phase noise performance [15].

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Furthermore, in the case of summed outputs, we discuss the phase alignment tolerances necessary to avoid AM-to-PM and PM-to-AM noise conversion, which are crucial for successfully enhancing the residual noise performance. This technique can be used to surpass the state-of-the-art regenerative dividers by simply adding enough DDS outputs, and at the same time the capability of dividing the input reference signal by any factor is retained without circuit redesign.

Section II demonstrates how power-combining multiple DDS sources with similar noise performance improves both phase and amplitude noise. The formulas to compute AM-to-PM and PM-to-AM conversion due to phase misalignment and a method for making residual measurements using an absolute noise analyzer and the carrier suppression technique [16] are presented in Section III. The same methods and formulas described in Sections II and III can be reused to improve the overall phase and amplitude noise on all types of signals, as long as they are generated from independent sources, and they can be added coherently. Section IV presents the realized hardware and the techniques implemented to guarantee a known phase relationship between each DDS output. Section V outlines the measurement setup, while Section VI describes the phase alignment procedure developed to ensure almost perfect signal addition. Finally, Section VII presents the exceptional residual phase noise performance obtained in our measurements.

II. Noise Reduction in Array of Parallel DDS

The model for a noisy sinusoidal signal in complex Euler form is

$$v(t) = V_0(1 + \alpha_m(t))e^{j(\omega_0 t + \varphi_m(t))} + n(t). \tag{1}$$

Here, V_0 and ω_0 represent the amplitude and angular frequency, respectively. $\alpha_m(t)$, $\varphi_m(t)$, and $n(t)$ are the stochastic processes that represent multiplicative fractional amplitude noise, multiplicative phase noise, and additive white noise, respectively. The choice of using a complex Euler versus a real sinusoid representation for the analytical analysis was made solely to simplify the equations. A modification to adapt the analysis to real signals will be presented later in the text. Assuming that the noise variables are small relative to the amplitude, one can simplify (1) as follows:

$$v(t) = V_0(1 + \alpha_m(t) + j\varphi_m(t))e^{j\omega_0 t} + n(t). \tag{2}$$

For a DDS, the additive white noise is typically generated by quantization and thermal noise, and we assume the thermal noise to be dominant over quantization noise. To determine the contribution of additive noise to AM and PM, we rewrite (2) as follows:

$$\begin{aligned} v(t) &= V_0\left(1 + \alpha_m(t) + j\varphi_m(t) + \frac{n(t)}{V_0}e^{-j\omega_0 t}\right)e^{j\omega_0 t} \\ &= V_0\left[1 + \alpha_m(t) + \frac{n(t)}{V_0}\cos(\omega_0 t) + j\varphi_m(t) \right. \\ &\qquad \left. - j\frac{n(t)}{V_0}\sin(\omega_0 t)\right]e^{j\omega_0 t}. \end{aligned} \tag{3}$$

The real and imaginary terms of (3) are represented as

$$\alpha = \alpha_m(t) + \frac{n(t)}{V_0}\cos(\omega_0 t), \quad \varphi = \varphi_m(t) - \frac{n(t)}{V_0}\sin(\omega_0 t). \tag{4}$$

Here, α represents the total (multiplicative plus additive) fractional amplitude fluctuations, and φ represents total phase fluctuations. Since the power spectral densities (PSDs) of AM and PM noise typically contain both multiplicative and additive components, we represent the additive noise from the carrier's point of view, by bringing it inside the complex exponential prior to calculating the PSD. Equation (4) shows that the power for the additive noise n is evenly split between AM and PM and it is true also for a real signal, even if (4) will be different.

As shown in Appendix A, using the Wiener–Khintchine theorem we are able to write the PSD of amplitude and phase fluctuations as

$$\begin{aligned} S_\alpha(\omega) &= S_{\alpha_m}(\omega) + \frac{S_n}{2V_0^2} \\ S_\varphi(\omega) &= S_{\varphi_m}(\omega) + \frac{S_n}{2V_0^2} \end{aligned} \tag{5}$$

where S_α, S_φ, S_{α_m}, S_{φ_m}, and S_n represent the PSD of the total AM noise, PM noise, multiplicative AM noise, multiplicative PM noise, and additive white noise, respectively. The white additive noise term in (5) needs to be modified when the complex Euler representation in (1) is substituted with a real sinusoid. All the PSD equations shown in this article can be modified for real sinusoidal signals $v(t) = \sqrt{2}V_0(1 + \alpha_m(t))\cos(\omega_0 t + \varphi_m(t)) + n(t)$ by doubling the terms containing S_n in (5), and by constraining α_m and φ_m bandwidths to $<\omega_0$.

Combining multiple in-phase independent signal sources, such as DDSs, allows for overall residual PM and AM noise reduction. A set of k independent sources with independent noise processes can be represented as

$$v_i(t) = V_0\left[1 + \alpha_{m_i}(t) + j\varphi_{m_i}(t)\right]e^{j\omega_0 t} + n_i(t), \quad \text{where } i = 1, 2, \ldots, k. \tag{6}$$

All the sources are assumed to have the same amplitude V_0. Signals with different output powers will result in a nonideal noise reduction case. Equations in Section III address the case of combining signals with different amplitudes for $k = 2$ signals. The same section also discusses the effect of phase misalignment between the combined signals.

Using a scattering matrix, M_S, the output signal of an ideal Wilkinson power splitter/combiner with k ports can be written as

$$\underbrace{\frac{-j}{\sqrt{k}}\begin{bmatrix} 0 & 1 & 1 & \cdot & 1 \\ 1 & 0 & 0 & \cdot & 0 \\ 1 & 0 & 0 & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ 1 & 0 & 0 & \cdot & 0 \end{bmatrix}}_{M_S}\begin{bmatrix} 0 \\ v_1(t) \\ v_2(t) \\ \cdot \\ v_k(t) \end{bmatrix} = \begin{bmatrix} v_\Sigma(t) \\ 0 \\ 0 \\ \cdot \\ 0 \end{bmatrix}. \tag{7}$$

Other power splitters/combiners can be used, and a Wilkinson type is presented because of its low-loss, high isolation,

and simpler scattering matrix. Using (6) and (7), the output of the power combiner, $v_\Sigma(t)$, can be written as

$$v_\Sigma(t) = \frac{-j}{\sqrt{k}}\left[V_0\left(k + \sum_{i=1}^{k}\alpha_{m_i}(t) + j\sum_{i=1}^{k}\varphi_{m_i}(t)\right)e^{j\omega_0 t} + \sum_{i=1}^{k} n_i(t)\right]. \quad (8)$$

For simplicity, we assume that the noise power of the random variables for all k signals is equal and therefore has the same PSD. Since the correlated signal amplitude adds linearly, and in contrast, the average power of the uncorrelated noise variables adds, the PSD of (8) results in

$$S_\alpha(\omega) = \frac{S_{\alpha_m}(\omega)}{k} + \frac{S_n}{2kV_0^2}$$
$$S_\varphi(\omega) = \frac{S_{\varphi_m}(\omega)}{k} + \frac{S_n}{2kV_0^2}. \quad (9)$$

Here, we show that for AM and PM both the multiplicative and additive noise powers are reduced by a factor k for the combined output versus the single output.

To highlight how the result in (9) can only be obtained if the signal sources are independent, we compare it with an array of amplifiers [17]. In this case, a single signal is first split in a power splitter to generate a set of k copies of the input signal. For an ideal case, one can write

$$\underbrace{\frac{-j}{\sqrt{k}}\begin{bmatrix} 0 & 1 & 1 & \cdot & 1 \\ 1 & 0 & 0 & \cdot & 0 \\ 1 & 0 & 0 & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ 1 & 0 & 0 & \cdot & 0 \end{bmatrix}}_{M_S}\begin{bmatrix} V_0 e^{j\omega_0 t} \\ 0 \\ 0 \\ \cdot \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ v_1(t) \\ v_2(t) \\ \cdot \\ v_k(t) \end{bmatrix}. \quad (10)$$

Each $v_i(t)$ signal is separately amplified with k independent amplifiers with voltage gain G and noise figure F, given by

$$v_{G_i}(t) = \frac{-j}{\sqrt{k}}\left[GV_0\left(1 + \alpha_{g_i}(t) + j\varphi_{g_i}(t)\right)e^{j\omega_0 t}\right] + G\sqrt{F}n_{g_i}(t), \quad \text{where } i = 1, 2, \ldots, k \quad (11)$$

where α_g, φ_g, and $\sqrt{F}n_g$ represent the flicker amplitude, flicker phase, and thermal noise contributions of the amplifiers, respectively. The same gain G and noise figure F are considered in all the amplifiers for simplicity. Variations in amplifier parameters will result in a nonideal summation and degraded phase and amplitude noise reduction. The k signal paths are now combined in a power combiner as above in (7) resulting in

$$v_\Sigma(t) = GV_0\left(1 + \frac{1}{k}\sum_{i=1}^{k}\alpha_{g_i}(t) + j\frac{1}{k}\sum_{i=1}^{k}\varphi_{g_i}(t)\right)e^{j\omega_0 t - \pi} - j\frac{G\sqrt{F}}{\sqrt{k}}\sum_{i=0}^{k} n_{g_i}(t). \quad (12)$$

The corresponding phase and amplitude noise for the amplifier array is

$$S_\alpha(\omega) = \frac{S_{\alpha_g}(\omega)}{k} + \frac{FS_{n_g}}{2V_0^2}$$
$$S_\varphi(\omega) = \frac{S_{\varphi_g}(\omega)}{k} + \frac{FS_{n_g}}{2V_0^2}. \quad (13)$$

Here, we can see that in contrast to (9), the additive thermal noise is not reduced by the factor k for the amplifier array, while the multiplicative amplitude and phase noise is.

In summary, for a parallel configuration of DDSs, both flicker noise and additive thermal noise improve, whereas for parallel amplifiers, only the flicker noise improves while the additive noise due to the amplifier's noise figure does not. This difference can be explained because, even though the uncorrelated additive thermal noise power of the individual amplifiers combines incoherently, the signal-to-noise gain at the output combiner is canceled by the signal-to-noise loss at the input power splitter.

III. Carrier Suppression and Noise Conversion

Low noise levels can be difficult to measure since measurement systems need to perform better than the device under test, or advanced techniques should be used. Since amplitude control and 180° phase inversions can be achieved via digital parameter adjustments in the DDS, we can easily implement a carrier suppression technique [16] for improving sensitivity and dynamic range of the noise measurements. By power-combining one DDS's output with another that is phase-inverted, we reduce the output power of the combined carrier which effectively increases the residual AM and PM noise, making it easier to measure. This carrier suppression also reduces the common-mode clock noise in the combined signal by the same amount, effectively converting an absolute measurement into a residual one. However, when two signals are combined, the relative phase between them must be carefully controlled; otherwise, AM noise in the individual signals can convert into PM noise in the combined output and vice versa.

To model carrier suppression, we sum two similar signals $v_1(t)$ and $v_2(t)$ with a Wilkinson power combiner

$$v_1(t) = V_0(1 + \alpha_1(t) + j\varphi_1(t))e^{j\omega_0 t} + n_1(t)$$
$$v_2(t) = \varepsilon V_0(1 + \alpha_2(t) + j\varphi_2(t))e^{j(\omega_0 t + \theta)} + n_2(t) \quad (14)$$

and the summed signal $v_\Sigma(t)$ is then written as

$$v_\Sigma(t) = \frac{-j}{\sqrt{2}}(v_1 + v_2). \quad (15)$$

Here, ε, is an amplitude scaling factor which can also be negative to implement carrier suppression, and θ represents the angle deviation from perfect addition or subtraction of the two signals. When $\varepsilon = 1$ and $\theta = 0$, the power-combined summation signal is equivalent to (8) for $k = 2$. Carrier suppression will occur when ε is between -1 and 0.

Using a first-order Taylor expansion around $\theta = 0$, we simply rewrite (15) as

$$v_\Sigma(t) = \frac{V_0(1+\varepsilon)}{\sqrt{2}}e^{j\left(\omega_0 t + \frac{\varepsilon\theta}{\varepsilon+1} - \frac{\pi}{2}\right)}(1 + \alpha_\Sigma + j\varphi_\Sigma). \quad (16)$$

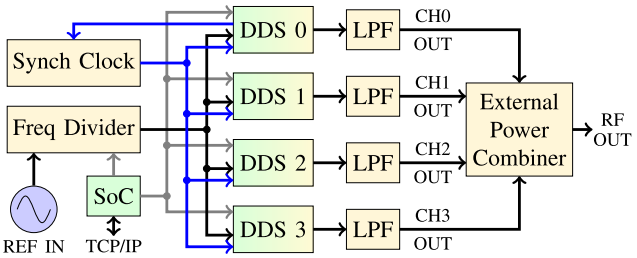


Fig. 1. Block diagram of the four-channel DDS board. SoC—Zynq SoC FPGA. LPF—low-pass filter. DDS = Analog Devices, AD9914, frequency divider = Analog Devices, HMC862A, synch clock = Analog Devices, LT6957-3.

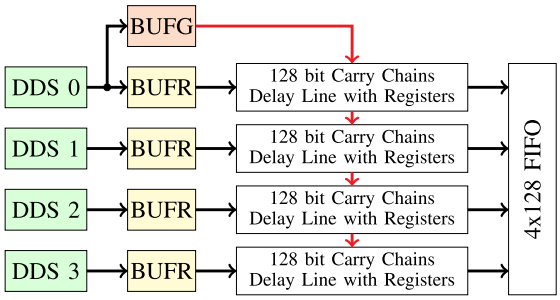


Fig. 2. Block diagram of the TDC. Regional clock buffers (BUFR) in the same clock region are used to ensure equal delay to the carry chain line inputs. Channel 0 is also connected to a global clock buffer (BUFG) with a ~1 ns increased delay with respect to the BUFRs, and it is used to clock all the registers in the delay lines at the same time. This allows to sample the signals propagating through the carry chain lines. A 128-bit delay line is made by combining 32 CARRY4 modules in the same FPGA logic column.

The corresponding amplitude and phase terms for the summed signal are given by

$$\alpha_\Sigma = \left(\frac{\alpha_1(t) + \varepsilon\alpha_2(t)}{\varepsilon+1} + \frac{\theta\varepsilon}{(\varepsilon+1)^2}(\varphi_1(t)+\varphi_2(t)) + \frac{\cos(\omega_0 t)}{V_0(\varepsilon+1)}(n_1(t)+n_2(t)) \right)$$

$$\varphi_\Sigma = \left(\frac{\varphi_1(t) + \varepsilon\varphi_2(t)}{\varepsilon+1} + \frac{\theta\varepsilon}{(\varepsilon+1)^2}(\alpha_1(t)+\alpha_2(t)) - \frac{\sin(\omega_0 t)}{V_0(\varepsilon+1)}(n_1(t)+n_2(t)) \right). \quad (17)$$

From (17), and assuming the pairs $\alpha_{1,2}$, $\varphi_{1,2}$, and $n_{1,2}$ have the same PSD, we can write the phase and amplitude noise spectra of the combined signal as

$$S_{\alpha_\Sigma}(\omega) = \frac{\varepsilon^2+1}{(\varepsilon+1)^2}S_\alpha(\omega) + \frac{2\theta^2\varepsilon^2}{(\varepsilon+1)^4}S_\varphi(\omega) + \frac{S_n}{V_0^2(\varepsilon+1)^2}$$

$$S_{\varphi_\Sigma}(\omega) = \frac{\varepsilon^2+1}{(\varepsilon+1)^2}S_\varphi(\omega) + \frac{2\theta^2\varepsilon^2}{(\varepsilon+1)^4}S_\alpha(\omega) + \frac{S_n}{V_0^2(\varepsilon+1)^2}. \quad (18)$$

Equations (16)–(18) are derived in Appendix B.

In this case, S_α, S_φ, and S_n refer to the amplitude, phase, and thermal noise of a single DDS, respectively, while S_{α_Σ} and S_{φ_Σ} refer to the phase and amplitude spectral densities of the combined output, respectively. Note that the scaling due to carrier suppression is not equal for additive and multiplicative noise for small values of suppression, $|\varepsilon| < 0.9$. When the input signals are not in perfect phase alignment ($\theta \neq 0$), amplitude noise is mapped to the phase quadrant and vice versa, as shown by the middle term of (18). A similar mapping of phase to amplitude also occurs. An expression for determining the angle that generates a specific AM-to-PM conversion ratio can be found by taking the ratio between the first and second terms in (18) for both lines

$$\theta = \sqrt{\frac{(\varepsilon^2+1)(\varepsilon+1)^2}{2\beta\varepsilon^2}} \quad (19)$$

where $\beta = S_\varphi/S_\alpha$ for PM-to-AM conversion or $\beta = S_\alpha/S_\varphi$ for AM-to-PM conversion.

Equations in (18) were rigorously tested and verified against Keysight Advanced Design System simulations.

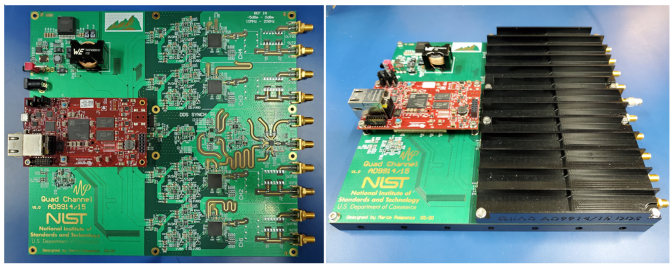
IV. Hardware and Software

The block diagram of the proposed design is presented in Fig. 1. The input periodic square wave, pulsed or sinusoidal reference signal (500 MHz–24 GHz), is digitally frequency divided by 1, 2, 4, or 8 to a maximum of 3.5 GHz using an Analog Devices HMC862A. The divider clock signal is then distributed to the four Analog Devices AD9914 DDSs chips through a clock distribution network. The clock division and distribution components' residual phase noise can be as high as −150 dBc/Hz for the white noise and −100 dBc/Hz for the 1-Hz flicker noise intercept [18], [19]. If the DDS division factor is larger than 32, the clock network's contribution is negligible at the output signal.

The first DDS chip (DDS 0) provides a square wave synchronization signal that is distributed to all the channels using two low-noise buffers. Using a custom FGPA-based measurement and software calibration procedure, synchronization of the DDS's state machines and phase accumulators for all the four channels is assured. Thus, a deterministic and well-known phase relationship between the outputs is achieved. Finally, the outputs are filtered with low-pass reconstruction filters.

An FPGA module featuring a Zynq-7000 [20] system on a chip (SoC) is used to control and monitor the synthesizer. The synchronization calibration procedure is implemented in FPGA and software, and the alignment between the channels is monitored by counting the SYNC_CLK front edges and their relative phase shift using a time-to-digital converter (TDC) implemented on the FPGA side of the SoC [21]. The block diagram of the TDC is shown in Fig. 2. Six 128-bit carry chain delay lines are used, two of which are used for calibration with an internally generated 350-MHz signal. The SYNC_CLK from DDS channel 0 (CH0) is used as a reference, which also drives the global clock buffer that samples the delay lines. Routing of each SYNC_CLK signal is done manually through regional clock buffers to ensure the same delay along the four channels from the FPGA pin to the carry chain input. All the six carry chain delay lines are manually placed to ensure close physical proximity to decrease ON-chip variation effects [22].

Since metastability in the sampling registers is present, 32 consecutive rising edges are measured and averaged. An overall resolution of 17 ps is achieved by counting the bits between transitions. A SYNC_CLK mismatch indicates a failure in the DDS's state machine synchronization, most likely caused by a synchronization signal violation of setup and hold



(a) (b)

Fig. 3. Designed four-channel DDS PCB. (a) Red PCB daughter board is the Microzed Zynq-7000 module, while the four AD9914 chips and the length matched clock transmission lines are clearly visible on the right side of the board. Each DDS output is on an SMA connector, and an optional 90° shifted version of it is available on a secondary SMA. The input reference is provided through the center SMA. (b) Completed assembly with the heatsink installed.

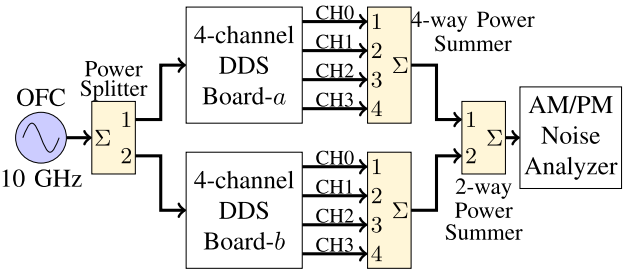


Fig. 4. Measurement block diagram. A single 10-GHz reference clocks two quad DDS boards, all the outputs are power-combined for a total of eight channels.

time requirements. In this case, the software resets the DDSs and tries a different combination of programmable delay lines built into the DDS chips. With this technique, we achieved synchronization of four AD9914 DDS chips clocked at their maximum speed of 3.5 GHz, a feature not advertised in the official datasheet [23], but present in the related part AD9915 [24] which can be clocked up to 2.5 GHz. The FPGA gateware and Linux software that runs on the SoC was created using the Koheron software development kit (SDK) [25]. A web server and interface running on the processor side of the SoC allow easy system control and monitoring though a local area network (LAN). Using a browser, the user can monitor SYNCH_CLK alignment and set DDSs words, phase, and amplitude parameters for any single AD9914 chip.

The photographs of the four-channel DDS printed circuit board (PCB) are shown in Fig. 3. A custom heat sink was machined as shown in Fig. 3(b) to keep the DDS chips at a more constant temperature, in part to the added thermal mass, and thus decreasing the effects of temperature variations on output stability. The input clock reference is distributed to the DDS chips using length-matched transmission lines. Furthermore, the SYNC_CLK signals from the DDS chips to the FPGA are length-matched because of their importance in monitoring system synchronization.

V. Measurement Technique

The block diagram of the multichannel DDS evaluation setup is shown in Fig. 4. The DDSs were clocked with a common 10-GHz signal provided by a cavity-stabilized 250-MHz fiber-based optical frequency comb (OFC).

The input clock is divided by 4 to provide 2.5 GHz to each DDS chip, which is further divided by 256 using the DDSs for a total division factor of 1024. This gives a spur-free [10] 9.765625 MHz output that can be used to measure the system phase noise performance.

The four output channels of each board are power-combined with a four-way Wilkinson power combiner. The two combiner outputs are then further merged with a two-way Wilkinson power combiner. Finally, the signal is sent to an AM/PM noise analyzer.

According to the theory described in Sections II and III, if all the channels ($k = 8$) are outputting the same in-phase signal, the final output amplitude increases by $\sqrt{k} = +9$ dB, and the phase noise of the eight-channel parallel DDS is expected to be 9 dB lower than a single channel [15].

For the PM and AM noise measurements, we used the Rohde and Schwarz FSWP50 noise analyzer. To reduce the dynamic range needed, we implemented a carrier suppression technique [16] in conjunction with the absolute noise measurement mode of the FSWP50. As shown in Section III, by suppressing the noise of the common carrier, we effectively measure the residual phase noise of the individual DDSs. This method also allowed us to effectively measure the residual noise in a single eight-channel DDS divider, rather than needing a pair of dividers that is required for a conventional residual divider noise measurement. The output carrier is suppressed in a controlled way by inverting the phase to 180° for one of the combined four-channel DDS boards.

With high levels of carrier suppression, an amplifier is typically necessary to restore the carrier power to a minimum level required by the measurement system. For our specific case, we can remove most of the absolute noise features by suppressing the +9 dBm carrier by ∼28 dB [Fig. 5(a), blue and lime color lines]. By choosing this moderate level of carrier suppression, we can avoid the use of an additional amplifier and its noise contributions while still meeting the −19 dBm minimum power requirement of the FSWP50 noise analyzer. The measurement process has the following steps.

1) Phase align all the channels as described in Section VI.
2) Flip the phase to 180° in all the channels in one of the two DDS boards.
3) Using the DDS output registers, slightly adjust the amplitude of the DDS channels to get the desired output power (∼−19 dBm to achieve the maximum measurable suppressed signal in our case). Measure accurately the output power P_{OS} in dBm.
4) Momentarily reflip the phase in one board to accurately measure the system output power P_O in dBm. The carrier suppression (P_S) can then be obtained from $P_S = P_{OS} - P_O$.
5) Perform an absolute AM or PM noise measurement of the suppressed carrier on FSWP50.
6) From (18), scale the measured multiplicative noise by $(\varepsilon^2 + 1)/((\varepsilon + 1)^2)$ to recover the noise of a single DDS board.
7) From (18), scale the measured thermal noise by $2/((\varepsilon + 1)^2)$ to recover the noise of a single DDS board. Here, the S_n term of (18) has already been corrected for a real

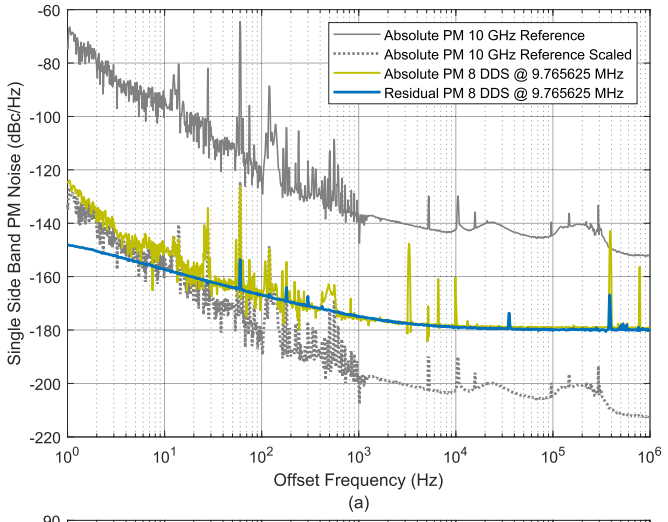


Fig. 5. (a) Absolute phase noise of the input reference at 10 GHz and power-combined output of the eight-channel synthesizer at 9.765625 MHz. The dotted gray line indicates the 10-GHz reference noise scaled to 9.765625 MHz as if divided noiselessly. The synthesizer output follows the scaled 10-GHz noise below an offset of 30 Hz, and dominated by the residual noise of the synthesizer at higher offsets. (b) Absolute and residual AM measurements overlap for most offset frequencies, since DDS outputs are independent of the reference's AM noise.

signal as opposed to the complex Euler form used in Sections II and III.

Since we measured the suppression as a ratio between the additive and suppressed powers of the synthesizer, $P_S = -28$ dB corresponds to a $\varepsilon = -0.92$. The relationship between P_S and ε is given as

$$\frac{1+\varepsilon}{1-\varepsilon} = 10^{\frac{P_S}{20}}. \tag{20}$$

VI. Phase Alignment

An initial residual phase and amplitude noise measurement of the AD9914 chip using only two DDS outputs was performed. The AM noise was almost 38 dB higher than the PM noise, as shown in Fig. 6.

This high level of AM noise requires a careful alignment of the phase of all the channels to prevent AM-to-PM conversion

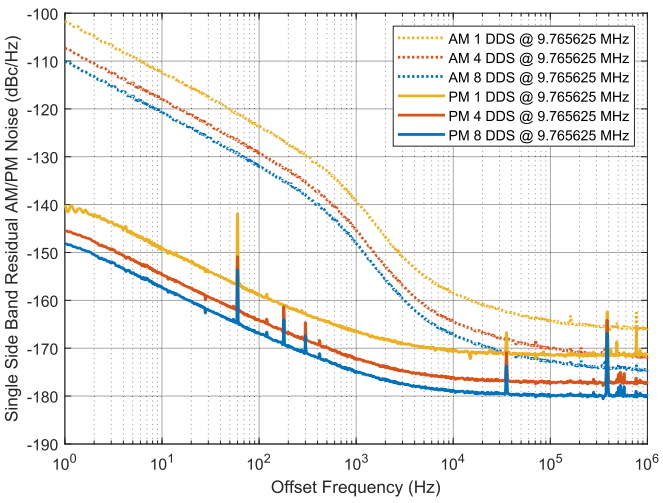


Fig. 6. Residual phase and amplitude noise of the power-combined output for one-, four-, and eight-channel synthesizer at 9.765625 MHz. 3 dB improvements in both AM and PM noise are visible when the number of channels combined is doubled. The 400-kHz spur and its harmonics are due to a switching power supply in the system.

in the combined signal. For $\varepsilon = -0.92$ and $\beta = 53$ dB, we can show from (19) that we need to control the phase angle, θ, between input signals to less than 0.011°. Here, the value for β was chosen by adding 15 dB to the measured AM/PM noise ratio of a single DDS to minimize the bias from DDS AM noise. At the generated frequency of 9.765625 MHz, this phase shift translates to a tolerance of about ∼0.5 mm for PCB trace length and cables. This tight constraint made us develop the following alignment procedure to ensure negligible AM noise leakage to PM when adding two or more channels together.

1) Connect power combiners and torque all the connectors.
2) Turn on the system, feed the reference signal, and let it warm up.
3) Perform a synchronization calibration procedure on all the DDS boards and set the output frequency.
4) Turn off all the channels y using the amplitude register and/or the OSK feature in the DDS chips.
5) For each DDS board:
   a) Turn on channel 0 to full power and off all other channels.
   b) Turn on channel 1, add a phase shift of π.
   c) Using a spectrum analyzer or power meter, get the smallest amplitude possible by tuning the phase and amplitude registers.
   d) Add π to channel 1 and set full amplitude.
   e) Repeat 5a, 5b, 5c, and 5d for channels 2 and 3.
6) Phase align different boards using a similar procedure described in 4 and 5 using channel 0 s. Note that when the system is turned on, the boards have a random phase relation to each other. Use board a as a reference and adjust channel 0 of board b. Once channel 0 of board b is aligned to channel 0 of board a, add the phase shift found to all other channels of board b.
7) Repeat step 6 for each DDS board.
8) Turn on all the channels to full power.

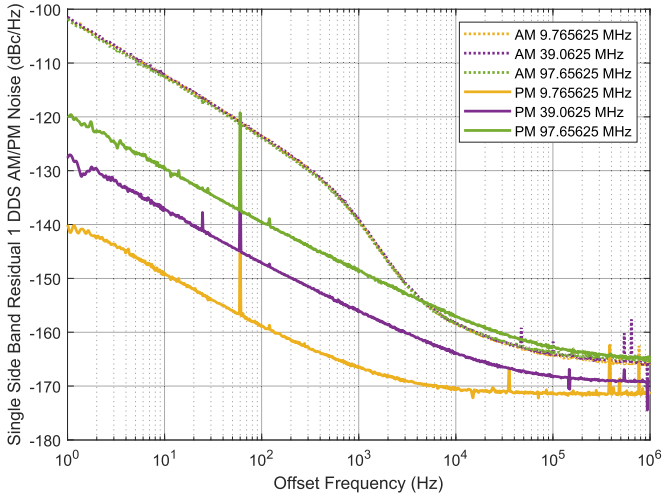


Fig. 7. Residual phase and amplitude noise of the power-combined output for the one-channel synthesizer at 9.765625, 39.0625, and 97.65625 MHz. PM noise scales as 20log(N) as expected, while the AM noise stays constant.

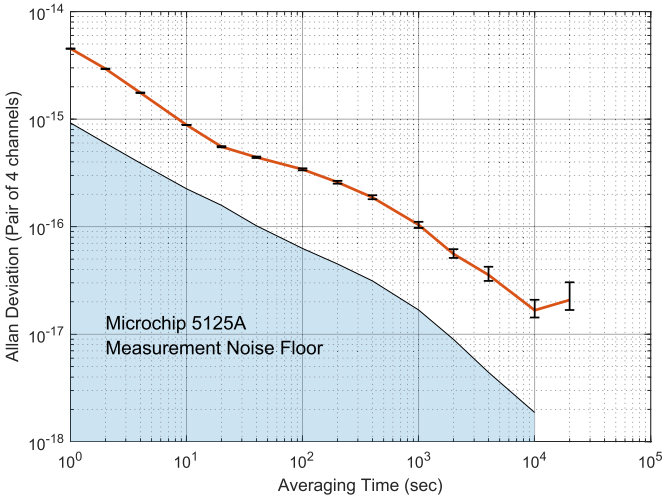


Fig. 8. Residual Allan deviation of a pair of four-channel DDS measured at 9.765625 MHz. For a single four-channel DDS, the Allan deviation is a factor of $\sqrt{2}$ less.

The procedure described ensures close-to-perfect phase alignment between all the channels, and it is feasible due to the 16-bit phase register in the DDS chips, which enables up to about 0.005° of angle resolution.

Furthermore, due to the high level of AM in the DDSs, there may be additional AM-to-PM conversion in the measurement system (FSWP50) that we did not compensate for in this measurement.

The measurement and phase alignment procedures described above have been created and tuned specifically for the system presented. However, they can be generalized to other systems as long as fine amplitude and phase control and 180° phase inversion are features available for each output source.

VII. Measurement Results

The residual phase and amplitude noise at 9.765625 MHz is depicted in Fig. 6 for one, four, and eight combined outputs. It shows that the flicker noise and white noise scale by 3 dB every time the combined outputs are doubled. A residual white phase noise level of −180 dBc/Hz is achieved with an array of eight parallel DDSs. For the array of DDSs, the flicker noise and white AM noise also decrease following the same behavior of $-10\log_{10}(k)$, where k is the number of combined outputs.

Fig. 5(a) shows the absolute phase noise of the 10-GHz reference signal (solid gray curve), its phase noise as if noiselessly frequency divided to 9.765625 MHz (dotted gray curve), and the eight-channel DDS output at 9.765625 MHz (solid lime curve). The residual phase noise (in solid blue) of the array DDS is also shown for comparison. The close-to-the-carrier phase noise demonstrates an ideal division (dotted gray curve) of the input reference, and above ∼30 Hz offset the synthesizer starts to be dominated by the residual noise of the DDSs and eventually reaches an absolute noise of −180 dBc/Hz. On the other hand, most AM noise from the reference does not transfer to the outputs [Fig. 5(b)] since the signal is regenerated digitally through the DDS output drivers. For this reason, the DDS absolute AM noise does not follow the 10-GHz reference AM noise.

Moreover, the ideal division behavior has been verified by measuring the residual phase and amplitude noise at different frequencies for 1 DDS output in Fig. 7. While the AM noise does not scale, the flicker phase noise is scaled according to theory by $-20\log_{10}(N)$, where N is the division factor between two frequencies.

Finally, Fig. 8 shows the residual Allan deviation for a pair of four-channel DDS boards. The system reaches a stability of 5×10^{-15} at 1 s, and 2×10^{-17} at 10 000 s of averaging time. The frequency stability was measured at 9.765625 MHz using the Microchip 5125A time-domain analyzer. The measurement configuration was similar as shown in Fig. 4, and the two signals for the measurement system were taken from the output of the two four-way power combiner.

VIII. Conclusion

A compact, general-purpose, four-channel DDS board is presented. We achieved single sideband residual phase noise of $\mathcal{L}(1\text{ Hz}) = -147$ dBc/Hz and $\mathcal{L}(100\text{ kHz}) = -180$ dBc/Hz at 9.765625 MHz by combining the outputs of eight synchronized DDSs. These phase noise levels are either comparable or lower than our previously reported result [13]. The residual noise measurements were performed with an absolute noise analyzer (Rohde and Schwarz FSWP50) in conjunction with carrier suppression and a low-noise 10-GHz clock signal. This clock was generated from a cavity-stabilized OFC that allowed us to synthesize an ultralow-noise 9.765625-MHz signal with an absolute white phase noise of −180 dBc/Hz. However, the absolute phase noise at the 1-Hz frequency offset was limited by the frequency comb noise and did not reach the −147 dBc/Hz residual noise level of the synthesizer. Analysis of AM and PM noise improvements due to an array of parallel DDSs is provided. In addition, an expression for phase-alignment tolerance to prevent AM-to-PM conversion during power-combining of signals has been derived and discussed.

APPENDIX A
SUM OF NOISE PROCESSES

The noise processes $\alpha_m(t)$, $\varphi_m(t)$, and $n(t)$ are summed as follows:

$$\alpha = \alpha_m(t) + \frac{n(t)}{V_0}\cos(\omega_0 t), \quad \varphi = \varphi_m(t) - \frac{n(t)}{V_0}\sin(\omega_0 t). \tag{21}$$

According to the Wiener–Khintchine theorem for wide-sense-stationary random process, the one-sided dual power spectral density (PSD) is computed as

$$S_\alpha(\omega) = 2\mathcal{F}\{r_{\alpha\alpha}(\tau)\}, \quad S_\varphi(\omega) = 2\mathcal{F}\{r_{\varphi\varphi}(\tau)\} \tag{22}$$

where the operator $\mathcal{F}$ represents the Fourier transform, and $r_{\alpha\alpha}(\tau) = \mathbb{E}[\alpha^*(t)\alpha(t-\tau)]$ and $r_{\varphi\varphi}(\tau) = \mathbb{E}[\varphi^*(t)\varphi(t-\tau)]$ are the autocorrelation functions.

Equation (21) can be rewritten as

$$\begin{aligned}\alpha(t) &= \alpha_m(t) + \frac{n(t)}{2V_0}e^{j\omega_0 t} + \frac{n(t)}{2V_0}e^{-j\omega_0 t}\\ \varphi(t) &= \varphi_m(t) - \frac{n(t)}{2jV_0}e^{j\omega_0 t} + \frac{n(t)}{2jV_0}e^{-j\omega_0 t}\end{aligned} \tag{23}$$

and the autocorrelation function $r_{\alpha\alpha}(\tau)$ can be found

$$\begin{aligned}&r_{\alpha\alpha}(\tau)\\ &= \mathbb{E}[\alpha_m(t)\alpha_m(t-\tau)] + \cancelto{0}{\mathbb{E}\left[\alpha_m(t)\frac{n(t-\tau)}{2V_0}e^{j\omega_0(t-\tau)}\right]}\\ &\quad + \cancelto{0}{\mathbb{E}\left[\alpha_m(t)\frac{n(t-\tau)}{2V_0}e^{-j\omega_0(t-\tau)}\right]}\\ &\quad + \cancelto{0}{\mathbb{E}\left[\frac{n(t)}{2V_0}e^{-j\omega_0 t}\alpha_m(t-\tau)\right]}\\ &\quad + \mathbb{E}\left[\frac{n(t)}{2V_0}e^{-j\omega_0 t}\frac{n(t-\tau)}{2V_0}e^{j\omega_0(t-\tau)}\right]\\ &\quad + \mathbb{E}\left[\frac{n(t)}{2V_0}e^{-j\omega_0 t}\frac{n(t-\tau)}{2V_0}e^{-j\omega_0(t-\tau)}\right]\\ &\quad + \cancelto{0}{\mathbb{E}\left[\frac{n(t)}{2V_0}e^{j\omega_0 t}\alpha_m(t-\tau)\right]}\\ &\quad + \mathbb{E}\left[\frac{n(t)}{2V_0}e^{j\omega_0 t}\frac{n(t-\tau)}{2V_0}e^{j\omega_0(t-\tau)}\right]\\ &\quad + \mathbb{E}\left[\frac{n(t)}{2V_0}e^{j\omega_0 t}\frac{n(t-\tau)}{2V_0}e^{-j\omega_0(t-\tau)}\right]\\ &= \mathbb{E}[\alpha_m(t)\alpha_m(t-\tau)] + \frac{1}{2V_0^2}\mathbb{E}\left[n(t)n(t-\tau)e^{j\omega_0\tau}\right]\\ &\quad + \cancelto{0}{\frac{1}{2V_0^2}\mathbb{E}\left[n(t)n(t-\tau)e^{j\omega_0(2t-\tau)}\right]}.\end{aligned} \tag{24}$$

Because $\alpha_m(t)$ and $n(t)$ are real and uncorrelated functions, terms where they are multiplied have zero expectation. The reason why $\mathbb{E}[n(t)n(t-\tau)e^{j\omega_0(2t-\tau)}] = 0$ is less intuitive, but it can be deducted from $\mathbb{E}[n(t)n(t-\tau)] = \delta(\tau)$ due to the nature of white noise. In fact, $\delta(\tau) = 1$ only for $\tau = 0$, and we have $n(t)n(t-0)e^{j2\omega_0 t}$ that has no expected value since $n^2(t)$ is being rotated over time and its energy spread evenly between positive and negative sides. Moreover, since $n(t)$ is defined as white noise, we have that $\mathbb{E}[n(t)n(t-\tau)e^{j\omega_0\tau}] = \mathbb{E}[n(t)n(t-\tau)]$, and its PSD will be constant in the entire spectrum.

Using a process similar to the one shown in (24), we also calculate $r_{\varphi\varphi}(\tau)$

$$\begin{aligned}r_{\alpha\alpha}(\tau) &= \mathbb{E}[\alpha_m(t)\alpha_m(t-\tau)] + \frac{1}{2V_0^2}\mathbb{E}[n(t)n(t-\tau)]\\ r_{\varphi\varphi}(\tau) &= \mathbb{E}[\varphi_m(t)\varphi_m(t-\tau)] + \frac{1}{2V_0^2}\mathbb{E}[n(t)n(t-\tau)]\end{aligned} \tag{25}$$

and they both convert to

$$\begin{aligned}S_\alpha(\omega) &= 2\mathcal{F}\{\mathbb{E}[\alpha_m(t)\alpha_m(t-\tau)]\} + \frac{1}{2V_0^2}2\mathcal{F}\{\mathbb{E}[n(t)n(t-\tau)]\}\\ S_\varphi(\omega) &= 2\mathcal{F}\{\mathbb{E}[\varphi_m(t)\varphi_m(t-\tau)]\} + \frac{1}{2V_0^2}2\mathcal{F}\{\mathbb{E}[n(t)n(t-\tau)]\}\end{aligned} \tag{26}$$

$$\begin{aligned}S_\alpha(\omega) &= S_{\alpha_m}(\omega) + \frac{S_n}{2V_0^2}\\ S_\varphi(\omega) &= S_{\varphi_m}(\omega) + \frac{S_n}{2V_0^2}.\end{aligned} \tag{27}$$

Note that $\alpha(t)$ lies on the real axis, while $\varphi(t)$ is on the imaginary, and according to the math shown in this appendix, their PSD stays orthogonal since autocorrelation functions have no imaginary part.

APPENDIX B
AM AND PM NOISE PROPAGATION IN POWER-COMBINED DDSS

The two signals $v_1(t)$ and $v_2(t)$ are considered

$$\begin{aligned}v_1(t) &= V_0(1 + \alpha_1(t) + j\varphi_1(t))e^{j\omega_0 t} + n_1(t)\\ v_2(t) &= \varepsilon V_0(1 + \alpha_2(t) + j\varphi_2(t))e^{j(\omega_0 t + \theta)} + n_2(t)\end{aligned} \tag{28}$$

where $\theta \approx 0$ and $\alpha_{1,2}$, $\varphi_{1,2}$, and $n_{1,2}$ represent, respectively, multiplicative amplitude, multiplicative phase, and thermal noise contributions.

First, we divide the thermal noise contribution into its orthogonal components as performed in Section II

$$\begin{aligned}v_1(t) &= V_0\left[1 + \alpha_1(t) + \frac{n_1(t)}{V_0}\cos(w_0 t) + j\varphi_1(t) - j\frac{n_1(t)}{V_0}\sin(w_0 t)\right]e^{j\omega_0 t}\\ v_2(t) &= \varepsilon V_0\left[1 + \alpha_2(t) + \frac{n_2(t)}{\varepsilon V_0}\cos(w_0 t + \theta) + j\varphi_2(t) - j\frac{n_2(t)}{\varepsilon V_0}\sin(w_0 t + \theta)\right]e^{j(\omega_0 t + \theta)}.\end{aligned} \tag{29}$$

The summed signal $v_\Sigma(t)$ using a Wilkinson power combiner is defined as

$$v_\Sigma(t) = \frac{-j}{\sqrt{2}}(v_1 + v_2) \tag{30}$$

and the expected final phasor can be easily found by removing all the noise contributions from (29)

$$\mathbb{E}[v_\Sigma] = \frac{-jV_0}{\sqrt{2}}\left(1 + \varepsilon e^{j\theta}\right)e^{j\omega_0 t}. \tag{31}$$

Using a first-order Taylor expansion, we can replace $e^{j\theta}$ with $1 + j\theta$, and covert the resulting complex number into polar form

$$\mathbb{E}[v_\Sigma] = \frac{-jV_0}{\sqrt{2}}\left(\sqrt{(1+\varepsilon)^2+\theta^2}\right)e^{j\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}}. \tag{32}$$

Since $\theta \approx 0$ is assumed, (32) can be simplified to

$$\mathbb{E}[v_\Sigma] = \frac{V_0(1+\varepsilon)}{\sqrt{2}}e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}-\frac{\pi}{2}\right)}. \tag{33}$$

The final result will have the form

$$v_\Sigma(t) = \frac{V_0(1+\varepsilon)}{\sqrt{2}}e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}-\frac{\pi}{2}\right)} + \frac{-j}{\sqrt{2}}\alpha_{\mathbb{E}} + \frac{-j}{\sqrt{2}}j\varphi_{\mathbb{E}} \tag{34}$$

where $\alpha_{\mathbb{E}}$ and $\varphi_{\mathbb{E}}$ are, respectively, the resulting AM and PM noise added to the expected phasor.

Now we can project all the four noise contributions for both v_1 and v_2 to the expected phasor $\mathbb{E}[v_1 + v_2] = V_0(\varepsilon + 1)e^{(j(\omega_0 t+\varepsilon\theta/(\varepsilon+1)))}$ [Fig. 9]. Note that the angle between the phasors $\mathbb{E}[v_1 + v_2]$ and v_1 is $(\varepsilon\theta)/(\varepsilon + 1)$, while the angle between $\mathbb{E}[v_1 + v_2]$ and v_2 is instead $\theta - (\varepsilon\theta)/(\varepsilon + 1) = \theta/(\varepsilon + 1)$.

$$\alpha_{\mathbb{E}}|_{v_1} = V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\alpha_1(t)\cos\dfrac{\varepsilon\theta}{\varepsilon+1}+\varphi_1(t)\sin\dfrac{\varepsilon\theta}{\varepsilon+1}\\ +\dfrac{n_1(t)}{V_0}\cos(\omega_0 t)\cos\dfrac{\varepsilon\theta}{\varepsilon+1}\\ -\dfrac{n_1(t)}{V_0}\sin(\omega_0 t)\sin\dfrac{\varepsilon\theta}{\varepsilon+1}\end{array}\right) \tag{35}$$

$$\alpha_{\mathbb{E}}|_{v_2} = V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\varepsilon\alpha_2(t)\cos\dfrac{\theta}{\varepsilon+1}+\varepsilon\varphi_2(t)\sin\dfrac{\theta}{\varepsilon+1}\\ +\dfrac{n_2(t)}{V_0}\cos(\omega_0 t+\theta)\cos\dfrac{\theta}{\varepsilon+1}\\ -\dfrac{n_2(t)}{V_0}\sin(\omega_0 t+\theta)\sin\dfrac{\theta}{\varepsilon+1}\end{array}\right) \tag{36}$$

$$\varphi_{\mathbb{E}}|_{v_1} = V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\alpha_1(t)\sin\dfrac{\varepsilon\theta}{\varepsilon+1}+\varphi_1(t)\cos\dfrac{\varepsilon\theta}{\varepsilon+1}\\ +\dfrac{n_1(t)}{V_0}\cos(\omega_0 t)\sin\dfrac{\varepsilon\theta}{\varepsilon+1}\\ -\dfrac{n_1(t)}{V_0}\sin(\omega_0 t)\cos\dfrac{\varepsilon\theta}{\varepsilon+1}\end{array}\right) \tag{37}$$

$$\varphi_{\mathbb{E}}|_{v_2} = V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\varepsilon\alpha_2(t)\sin\dfrac{\theta}{\varepsilon+1}+\varepsilon\varphi_2(t)\cos\dfrac{\theta}{\varepsilon+1}\\ +\dfrac{n_2(t)}{V_0}\cos(\omega_0 t+\theta)\sin\dfrac{\theta}{\varepsilon+1}\\ -\dfrac{n_2(t)}{V_0}\sin(\omega_0 t+\theta)\cos\dfrac{\theta}{\varepsilon+1}\end{array}\right). \tag{38}$$

With the assumption, $\theta \approx 0$ (35)–(38) can be simplified. In fact, we see that $\cos((\varepsilon\theta)/(\varepsilon + 1)) \approx 1$, $\cos(\theta/(\varepsilon + 1)) \approx 1$, $\sin((\varepsilon\theta)/(\varepsilon + 1)) \approx (\varepsilon\theta)/(\varepsilon + 1)$, $\sin(\theta/(\varepsilon + 1)) \approx \theta/\varepsilon + 1$, $\cos(\omega_0 t+\theta) \approx \cos(\omega_0 t)$ and $\sin(\omega_0 t+\theta) \approx \sin(\omega_0 t)$.

From an energy point of view, the following quantities dominate over others that will be neglected: $(n_1(t)/V_0)\cos(\omega_0 t))^2 \gg (n_1(t)/V_0)\sin(\omega_0 t)(\varepsilon\theta)/(\varepsilon + 1))^2$, $(n_2(t)/V_0)\cos(\omega_0 t))^2 \gg (n_2(t)/V_0)\sin(\omega_0 t)\theta/(\varepsilon + 1))^2$, $(n_1(t)/V_0)\sin(\omega_0 t))^2 \gg (n_1(t)/V_0)\cos(\omega_0 t)(\varepsilon\theta)/(\varepsilon + 1))^2$ and $(n_2(t)/V_0)\sin(\omega_0 t))^2 \gg (n_2(t)/V_0)\cos(\omega_0 t)\theta/(\varepsilon + 1))^2$.

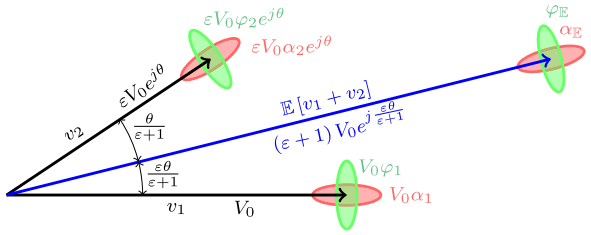


Fig. 9. Graphical representation of the noise conversion process.

Therefore, we get

$$\begin{aligned}\alpha_{\mathbb{E}} &= \alpha_{\mathbb{E}}|_{v_1} + \alpha_{\mathbb{E}}|_{v_2}\\ &\approx V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\alpha_1(t)+\varepsilon\alpha_2(t)+\dfrac{\theta\varepsilon}{\varepsilon+1}(\varphi_1(t)+\varphi_2(t))\\ +\dfrac{\cos(\omega_0 t)}{V_0}(n_1(t)+n_2(t))\end{array}\right)\\ \varphi_{\mathbb{E}} &= \varphi_{\mathbb{E}}|_{v_1} + \varphi_{\mathbb{E}}|_{v_2}\\ &\approx V_0 e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}\right)}\left(\begin{array}{l}\varphi_1(t)+\varepsilon\varphi_2(t)+\dfrac{\theta\varepsilon}{\varepsilon+1}(\alpha_1(t)+\alpha_2(t))\\ -\dfrac{\sin(\omega_0 t)}{V_0}(n_1(t)+n_2(t))\end{array}\right).\end{aligned} \tag{39}$$

When (34) is rearranged in the form

$$v_\Sigma(t) = \frac{V_0(1+\varepsilon)}{\sqrt{2}}e^{j\left(\omega_0 t+\frac{\varepsilon\theta}{\varepsilon+1}-\frac{\pi}{2}\right)}(1+\alpha_\Sigma+j\varphi_\Sigma) \tag{40}$$

we get instead

$$\begin{aligned}\alpha_\Sigma &= \left(\begin{array}{l}\dfrac{\alpha_1(t)+\varepsilon\alpha_2(t)}{\varepsilon+1}+\dfrac{\theta\varepsilon}{(\varepsilon+1)^2}(\varphi_1(t)+\varphi_2(t))\\ +\dfrac{\cos(\omega_0 t)}{V_0(\varepsilon+1)}(n_1(t)+n_2(t))\end{array}\right)\\ \varphi_\Sigma &= \left(\begin{array}{l}\dfrac{\varphi_1(t)+\varepsilon\varphi_2(t)}{\varepsilon+1}+\dfrac{\theta\varepsilon}{(\varepsilon+1)^2}(\alpha_1(t)+\alpha_2(t))\\ -\dfrac{\sin(\omega_0 t)}{V_0(\varepsilon+1)}(n_1(t)+n_2(t))\end{array}\right).\end{aligned} \tag{41}$$

Finally, we assume the pairs $\alpha_{1,2}$, $\varphi_{1,2}$, and $n_{1,2}$ having the same PSD, and we compute α_Σ and φ_Σ PSD as in Appendix A

$$\begin{aligned}S_{\alpha_\Sigma}(\omega) &= \frac{\varepsilon^2+1}{(\varepsilon+1)^2}S_\alpha(\omega)+\frac{2\theta^2\varepsilon^2}{(\varepsilon+1)^4}S_\varphi(\omega)+\frac{S_n}{V_0^2(\varepsilon+1)^2}\\ S_{\varphi_\Sigma}(\omega) &= \frac{\varepsilon^2+1}{(\varepsilon+1)^2}S_\varphi(\omega)+\frac{2\theta^2\varepsilon^2}{(\varepsilon+1)^4}S_\alpha(\omega)+\frac{S_n}{V_0^2(\varepsilon+1)^2}.\end{aligned} \tag{42}$$

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DISCLAIMER

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