A Sub-Sampling Digital PM/AM Noise Measurement System

Craig W. Nelson and David A. Howe

Abstract: A digital phase/amplitude modulation (PM/AM) noise measurement system (DNMS) implementing field programmable gate array (FPGA) based digital down converters (DDCs), and 250 MHz analog to digital converters (ADCs) is reported. Measurements in the first, baseband Nyquist region shows white phase noise floors of less than -180 dBc/Hz. With proper pre-filtering of the input signals to prevent undesired aliasing, high bandwidth track and hold amplifiers (THA) extend the operating range of the DNMS to microwave frequencies. Preliminary testing with an 18 GHz THA shows residual white phase noise floors at 10 GHz of less than -160 dBc/Hz.

1. Introduction

During the last decade, the digital phase noise measurement system (DNMS) has become a powerful tool that allows simple and accurate phase noise measurements to be accessible even for the neophyte. The differential measurement of phase between two oscillators with different frequencies, while not requiring a phase lock between the device under test (DUT) and the reference, has drastically simplified the process of making phase noise measurements. The complex analog frequency synthesis process needed to compare two signals with different frequencies can now be replaced with a simple mathematical scaling factor in the DNMS.

The basic building block of the DNMS is the digital down converter (DDC) [1, 2] shown in Figure 1. The DDC is a digital implementation of the traditional In-phase/Quadrature (I/Q) demodulator. The signal to be analyzed is digitized and multiplied by an I/Q reference generated from a numerical oscillator. The I and Q channels are filtered, and down-sampled to a convenient sample rate for mathematical analysis. A rectangular to polar conversion of the I and Q signals yields the phase and amplitude of the input signal. The instantaneous phase of the signal is computed directly in units of radians and no calibration factor is needed [3, 4]. However, because the carrier frequency is directly sampled by an analog-to-digital converter (ADC), one of the primary drawbacks of a DNMS is its limited frequency range of operation.

The modern implementation of the DNMS was created after a Small Business Innovation Research (SBIR) grant request was issued by National Institute of Standards and Technology (NIST) in 2003. This SBIR (SB1341-03-W-0817) was awarded to Timing Solutions Corporation (now part of Symmetricom, Inc.) and they implemented many important improvements to the standard digital down converter (DDC) configuration; primarily, cross-spectrum analysis and the suppression of common mode clock noise by the differential measurement between a DUT and a reference [5]. The commercial implementation consists of a four-channel system where the DUT and reference signals are differentially measured in two parallel measurement systems.

The common mode clock noise is suppressed by subtraction in each differential phase measurement. The non-common mode noise such as ADC quantization noise is suppressed by cross-spectrum analysis between the two measurement systems. A block diagram of this configuration is shown in Fig. 2.

2. Description of Basic Measurement System

The commercially available DNMS that evolved from the SBIR program is sufficient for most users, but our metrology needs at NIST require several additional features and capabilities as listed below:

- Dual reference capability
- Shorter measurement runs
- Higher carrier frequency
- Higher offset frequency analysis
- Lower noise floors
- Amplitude noise
- Control of all aspects of the measurement

The dual reference capability allows the DUT to be measured differentially against two independent signal references. The noise of these references is uncorrelated and can be suppressed by cross-correlation. To be able to implement these additional features and capabilities, a four-channel cross spectrum PM/AM measurement system was constructed at NIST. Each of the four channels digitizes its radio frequency (rf) carrier with a 250 MHz, 16 bit ADC. The four DDCs and decimation chains were implemented in field programmable gate arrays (FPGA). Cascaded integrator-comb

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(CIC) polyphase decimators [2, 4, 6] were used in the DDC and analysis chain. The cross spectrum fast-Fourier transforms (FFT) were calculated in a PCI eXtensions for Instrumentation (PXI) host computer that was interfaced to the FPGA. Figure 3 shows that the residual white phase noise floor of the DNMS at 10 MHz is less than -180 dBc/Hz.

The spectrum of a discrete sampled signal is periodic; therefore, with careful pre-filtering, we can take advantage of aliasing to down-convert signals that lie above the Nyquist frequency. The ADC's selected for our implementation have an analog bandwith of about 600 MHz that allows limited sub sampling into the third Nyquist region.

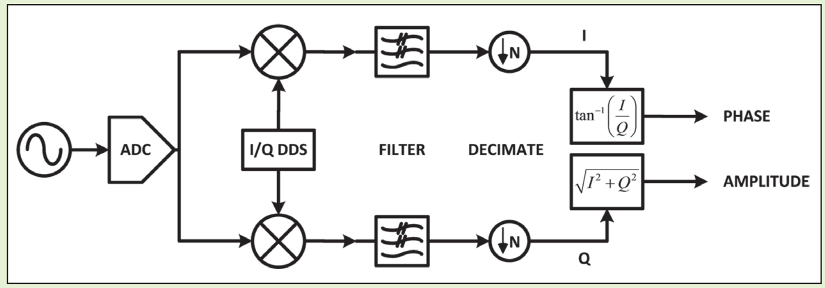

Figure 1. Block diagram for a digital down converter. Analog to digital converter (ADC), In-phase / Quadrature direct digital synthesizer (I/Q DDS).

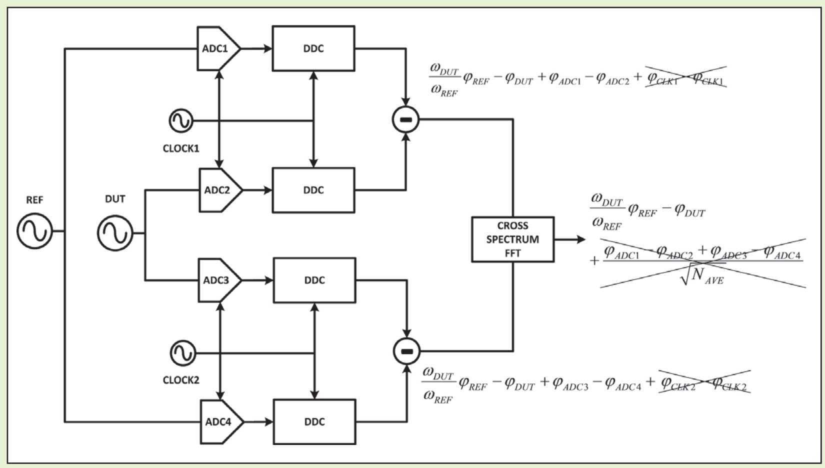

Figure 2. Block diagram of a four-channel DNMS. Reference source (REF), device under test (DUT), analog to digital converter (ADC), digital down- converter (DDC). w_x and φ_x are the angular frequency and phase of the reference or DUT. φ_{ADCn} represents the ADC quantization noise of channel n suppressed by the cross spectrum. φ_{CLKn} represents clock noise suppressed by common mode subtraction. N_{ave} is the number of averages in the cross spectrum calculation.

3. Track and Hold Frontend

To achieve digital PM/AM noise analysis at much higher frequencies than the 600 MHz available by the system described above, a track and hold analog sampling frontend was constructed for the DNMS. A block diagram of the front-end is shown in Figure 4. The track and hold amplifiers[7] with 18 GHz bandwidth and sampling rates of 4 GS/s were selected for the frontend. A fractional-N phase lock loop (PLL) synthesizer with an 18 MHz to 3 GHz tuning range was implemented as a common sampling clock for each THA pair. Careful delay matching of input, output and the clock transmission lines between each THA pair was made to ensure that common mode clock noise can be strongly rejected. Options for providing an external clock and additional clock outputs including a spread spectrum generator were also implemented. The spectrum clock modulator was not used or evaluated in this experiment. Figure 5 shows the block diagram of the completed sub-sampling digital measurement system utilizing a pair of dual THA modules, each with an independent sampling clock.

4. Performance

4.1. Residual Noise Tests

Residual SSB phase noise floor for the sub-sampling measurement system were made at 2, 10 and 18 GHz and are shown in Figure 6. The noise floors of $\mathscr{L}$ (thermal) = -160, -158 and -144 dBc/Hz and $\mathscr{L}$ (1 Hz) = -122, -110, -110 dBc/Hz were respectively achieved. Rejection of common mode clock noise via the differential phase measurement was as high as 60 dB. Non-rejected noise was due to non-correlated jitter in the clock circuitry of each individual THA. For these measurements the clock frequencies were chosen to produce a 10.7 MHz intermediate frequency at the output of the THA. 10 MHz was chosen due to the availability of convenient anti-alias filters. The DDC reference clock was set to produce a baseband signal at its output.

4.2. Absolute Noise Tests

Absolute phase noise measurements between a commercial synthesizer at three different frequencies and a fixed frequency dielectric resonator oscillator (DRO) at 10 GHz are shown in Figure 7. This showcases the capability to measure DUT and reference signals that are not phase locked and show a carrier frequency ratio as high as five. Independent verification of this measurement was made with a commercial phase noise analyzer and the results agreed to within ±1 dB with a slightly higher disagreement at a 100 kHz offset frequency. Figure 8 shows the same results all normalized to a carrier frequency of 10 GHz.

4.3. PM/AM Correlation Tests

Figure 9 shows simultaneous amplitude and phase noise measurements [8] along with the associated correlations between them. These types of correlations may be useful in the analysis of nonlinear oscillator optimization [9].

5. Conclusions

A four-channel 250 MS/s, 16 bit AM / PM digital noise measurement system was constructed and residual phase noise floors of $\mathscr{L}$(thermal) less than -180 dBc/Hz at 10 MHz were achieved. A four-channel track and hold frontend for the DNMS was demonstrated with extended measurement capabilities up

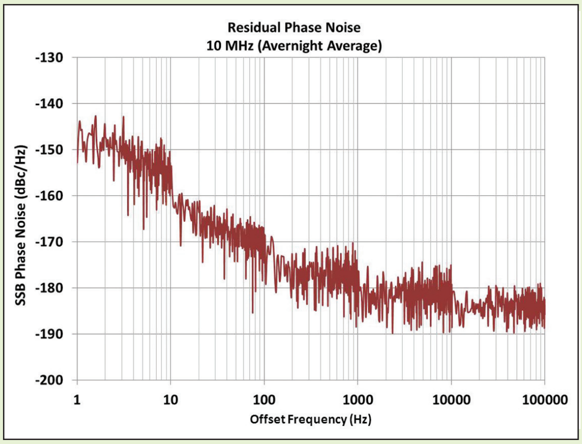

Figure 3. Residual single-sideband (SSB) phase noise floor of digital noise measurement system at 10 MHz. A single source at +15 dBm drives both the reference and device under test ports.

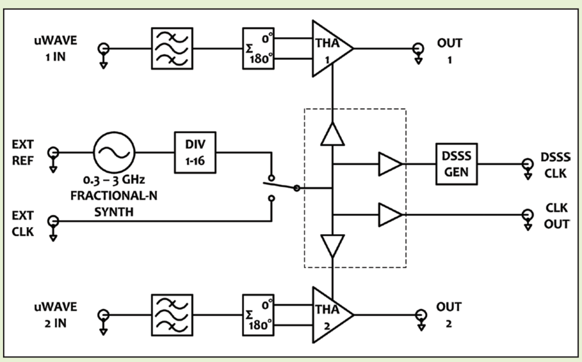

Figure 4. Dual track and hold with common fractional-N PLL sampling clock. Track and hold amplifier (THA), frequency divider (DIV 1-16), spread spectrum generator (DSSS GEN).

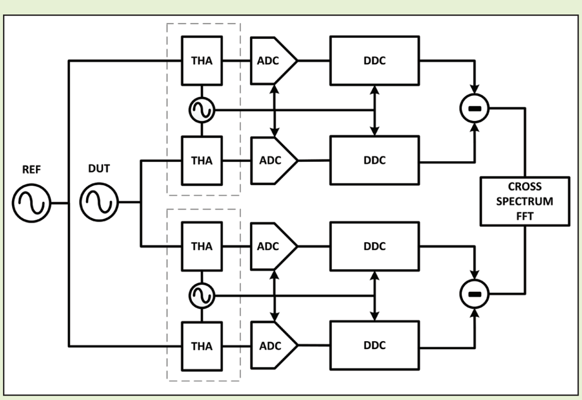

Figure 5. DNMS with track and hold frontend.

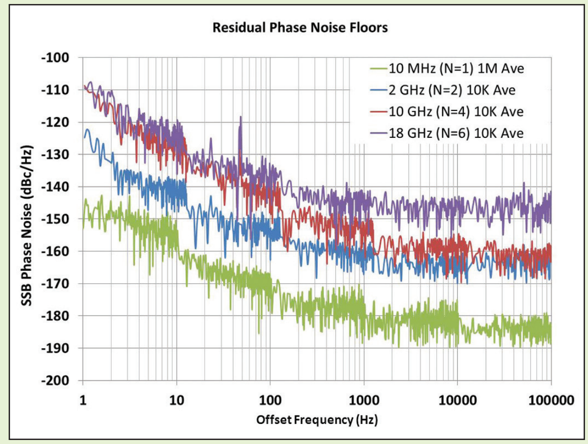

Figure 6. Residual SSB phase noise floor of the sub-sampling DNMS. N = Nyquist region, approximate sample rates = 125 MHz, 2 GHz, 2.5 GHz, and 3 GHz, averaging time is about 10 min.

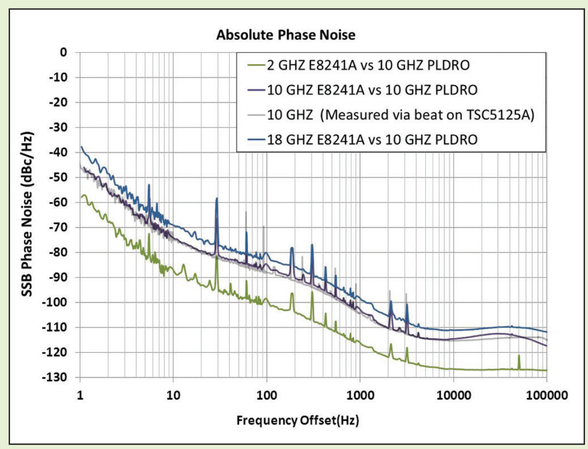

Figure 7. Absolute phase noise of E8241A synthesizer at three carrier frequencies versus a fixed 10 GHz phase locked DRO. Approximate sample rates = 2 GHz, 2.5 GHz, and 3 GHz, averaging time is ~10 min.

to 18 GHz. Future research involving the DNMS will include optical sampling [10] to extend the analysis of carrier frequencies out to 40 GHz, faster FPGA based FFT calculation, and moving to 12 bit, 3.6 GHz analog to digital converters.

6. Acknowledgements

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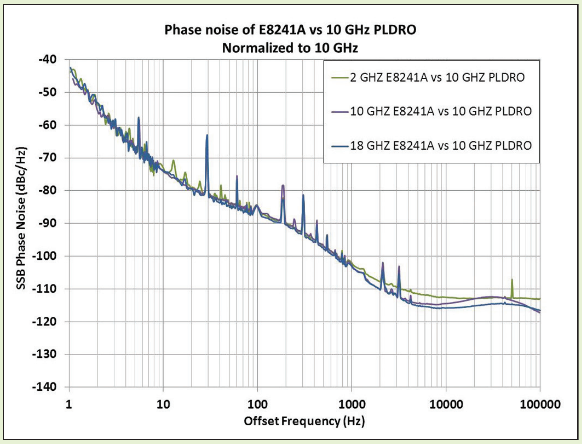

Figure 8. Absolute phase noise of E8241A synthesizer at three carrier frequencies versus a fixed 10 GHz phase locked DRO normalized to 10 GHz.

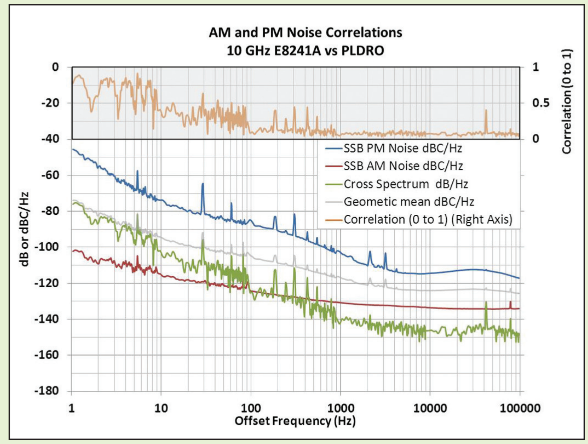

Figure 9. Amplitude and phase noise of synthesizer with correlation.

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