Automated High-Accuracy Phase Measurement System

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INTRODUCTION

THE MEASUREMENT of the accumulated phase or the time difference between pairs of clocks is required for timekeeping and is the most powerful method of making very accurate frequency measurements since time interval, frequency, and frequency difference may all be calculated from these measurements. In the past, frequency was usually not derived from time measurements for short sample times because the time measurements could not be performed with adequate precision. However, we have developed a new measurement system which overcomes this limitation. It combines the most advantageous properties of the three most common techniques: the heterodyne measurement system; the frequency divider; and the dual-mixer measurement system [1]. As a result, it can satisfy nearly any requirement for frequency or time measurement.

The new system has the low-noise and high-resolution properties of a single heterodyne system: the rms time deviation for a single measurement is typically 2 ps and the theoretical resolution is 0.2 ps for the particular design parameters we have chosen. But a single heterodyne system is seriously limited since it can only make a measurement at the time of a zero crossing between the oscillators under test, not at the time of the operators choice. As the result of the addition of a transfer oscillator, the new system, like the dual-mixer system, makes measurements within 0.1 s of any selected time and like a di-

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vider, the new measurement system stores the time of each clock in hardware and requires readout by a computer very infrequently. For example, no ambiguity occurs before 19 days have elapsed. The hardware utilizes the ANSI/IEEE-583 (CAMAC) interface standard to communicate with either a computer or desktop calculator in order to store and analyze data [2].

This paper discusses the theory of the measurement method, presents typical performance data, and outlines the important features of the computer operating system. Both the hardware and software could be adapted to a wide variety of measurement needs.

Hardware

This paper follows the IEEE recommendations for describing the phase noise in oscillators [3]. To account for the phase noise on a sine-wave signal generator, we express the output voltage as

$$V(t) = V_0 \sin [2\pi\nu_0 t + \phi(t)]$$

where

- V_0 nominal peak voltage amplitude
- ν_0 nominal fundamental frequency
- $\phi(t)$ deviation of phase from nominal

and amplitude variations have been assumed to be negligible.

The instantaneous frequency of the oscillator is the derivative of the phase divided by 2π

$$\nu(t) = \nu_0 + \frac{1}{2\pi}\frac{d\phi}{dt}.$$

It is useful to define a normalized frequency deviation

$$y(t) = \frac{\nu(t) - \nu_0}{\nu_0} = \frac{1}{2\pi\nu_0}\frac{d\phi}{dt}.$$

The integral of this normalized frequency is the time deviation $x(t)$ whose units are seconds

$$x(t+\tau) - x(t) = \int_t^{t+\tau} y(Z)\, dZ$$

and the average frequency deviation over the interval τ is defined as

$$\bar{y}(t+\tau; t) = \frac{1}{\tau}\int_t^{t+\tau} y(Z)\, dZ = \frac{x(t+\tau) - x(t)}{\tau}.$$

Frequency or phase measurements requiring the highest precision are always made by heterodyning the outputs from two oscillators using a suitable device such as a double-balanced mixer. Thus if the input signals are

$$V_1(t) = V_{10} \sin [2\pi\nu_{10} t + \phi_1(t)]$$

and

$$V_2(t) = V_{20} \cos [2\pi\nu_{20} t + \phi_2(t)]$$

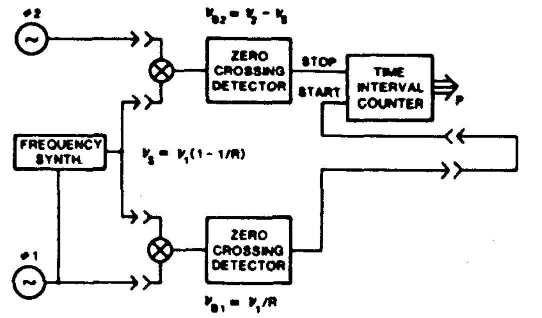

Fig. 1. Dual-mixer time difference measurement system.

then the low-pass filtered output of the mixer is

$$V_B(t) = V_{B0} \sin [2\pi(\nu_{20} - \nu_{10})t + \phi_2(t) - \phi_1(t)].$$

The advantage of heterodyning is that the magnitude of a phase fluctuations is preserved while the beat frequency is reduced by the heterodyne factor $\nu_{10}/(\nu_{20} - \nu_{10})$. Thus a given phase change corresponds to a larger time interval and may be measured with improved resolution and accuracy.

Various techniques are used to characterize the beat-frequency signal. The most powerful method is to sample the phase (or time deviation) at intervals of time equal to τ. This may be accomplished by measuring the time of the zero crossings. A device which does this permits time deviation measurements with subpicosecond resolution but requires an offset (beat) frequency. An additional disadvantage is that the measurement intervals must be multiples of the beat period.

Two heterodyne measurement systems which share a common oscillator may be combined to overcome this problem. A step was taken in this direction with the development of the dual-mixer time difference technique (Fig. 1) which measures the time difference between adjacent zero crossings of the two heterodyne frequencies. The common oscillator is synthesized from oscillator number 1. It is offset low by an amount large compared to the frequency difference between the oscillators under test. The start pulse occurs at time t_M when the common oscillator is in phase quadrature with oscillator number 1. The common oscillator constantly lags until at time t_N it is in phase quadrature with oscillator number 2 when the stop pulse is produced. The time interval counter registers P counts of its time base which has a period τ_c. The time deviation between oscillators 1 and 2 at time t_M is given by

$$x_2(t_M) - x_1(t_M) = -P\tau_c \bar{\nu}_{B2}(t_M; t_N)/\nu_{10}$$

where $\bar{\nu}_{B2}(t_M; t_N)$ signifies the average beat frequency over the time interval from t_M to t_N. Since this system uses adjacent zero crossings, it is insensitive to phase changes of a whole cycle between the oscillators.

To overcome this limitation, we have added two scalers to the basic measurement system, as shown in Fig. 2. The second time interval counter and the unused stop-signal output are added to make the two halves of the circuit identical, permitting the expansion of the system to measure any number of clocks. The difference in the scaler readings indicates the number of cycles which have elapsed between oscillators 1 and

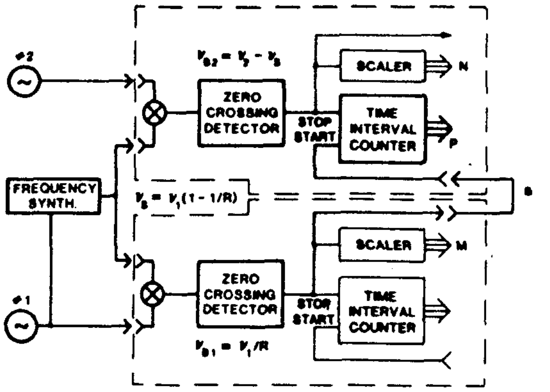

Fig. 2. Dual-mixer system extended for unambiguous time comparisons.

2 since the system was initialized. It can be shown that

$$x_2(t_M) - x_1(t_M) = [N - M - P\tau_c\bar{\nu}_{B2}(t_M; t_N)]/\nu_{10}$$

where N and M are the number of zero crossings of oscillators 2 and 1, respectively.

The average beat frequency $\bar{\nu}_{B2}(t_M; t_N)$ cannot be known exactly. However, it may be estimated with sufficient precision from the previous pair of measurements designated ′ and ″. The average frequency is approximately

$$\bar{\nu}_{B2}(t_M; t_N) \cong (N'' - N')/[R(M'' - M')/\nu_{10} + \tau_c(P'' - P')]$$

provided that it changes sufficiently slowly compared to the interval $t_M < t_N$. A typical value for this error will be given in the following section.

Performance

All measurement channels consist of a mixer, zero-crossing detector, scaler, and time-interval counter. Four such circuits can be built in a double-width CAMAC module. The system is easily expanded to compare many oscillators and the block diagram of a complete system for making phase comparisons among 24 clocks is shown in Fig. 3. We have chosen parameters which are reasonable for comparing state-of-the-art atomic standards. Thus the synthesizer is offset 10 Hz below oscillator 1 and $R = 5 \times 10^5$. The outputs from both mixers are approximately 10 Hz. The noise bandwidth is 100 Hz. The time base of the time interval counter is twice the frequency of oscillator 1 or approximately 10 MHz. The quantization error is $1/2R = 10^{-6}$ cycle or 0.2 ps which is a factor of ten smaller than the measurement noise. As stated earlier, an error will result from frequency changes which violate the constancy assumption used to estimate ν_{B2}. A change in ν_2 by 10^{-10} during the interval between two measurements will result in a time deviation error of 10 ps. Thus one must make more closely spaced measurements for oscillators which have large dynamic frequency changes than for more stable devices. Two other sources of inaccuracy are the sensitivities to the amplitude and phase of the common oscillator. Fig. 4 shows the measured value of $x = \phi/2\pi\nu_0$ as a function of the amplitude of the input signal and the phase of the synthesizer.

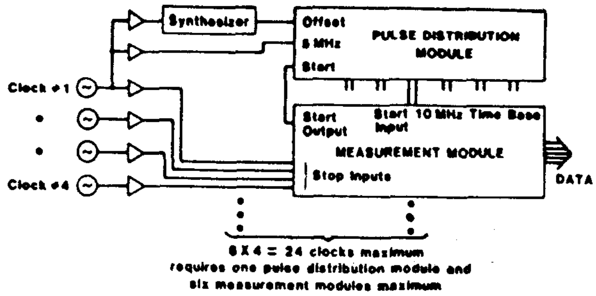

Fig. 3. Overall measurement system configuration.

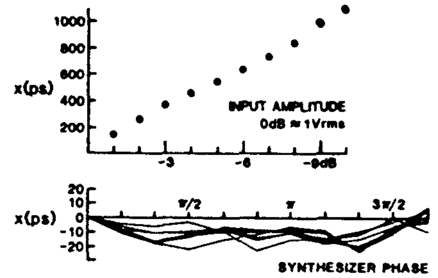

Fig. 4. Variations of measured time difference with important parameters.

The new measurement system has many desirable features and properties:

1) It has very high resolution, limited by the internal counters to 0.2 ps and by noise to approximately 2 ps.

2) It has much lower noise than divider-based measurement systems.

3) The operation is fully automatic.

4) All oscillators in the range of 5 MHz ± 5 Hz may be compared. Other carrier frequencies are also usable, but different carrier frequencies may not be mixed on the same system. The system has been successfully tested with an oscillator offset 4.6 Hz from nominal 5 MHz. Measurements were made at intervals of 2 h between which the system had to accumulate approximately $2 \times 10^6\pi$. The system has also been tested with an oscillator offset 4×10^{-9}, and no errors were detected during a period of 100 days.

5) All sampling times in the range of 1 s to 19 days with a resolution of 0.1 s are possible. Measurements may be made on command or in a preprogrammed sequence.

6) Measurements are synchronized precisely, i.e., at the picosecond level, with the reference clock. They may, therefore, be synchronized with important user system events, such as the switching times of an FSK or PSK system.

7) All oscillators are compared synchronously and all measurements are performed within a maximum interval of 0.1 s. As a result, the phase of an oscillator needs to be interpolated to the chosen measurement time for an interval of 0.1 s maximum. This capability, which is not present in either single heterodyne measurement systems or switched measurement systems eliminates a source of "measurement" error which is generally much larger than the noise-induced errors. For example, interpolation of the phase of a high-performance Cs clock ($\sigma_y \sim 10^{-11}/\tau^{1/2}$) over a period of 3 h would produce

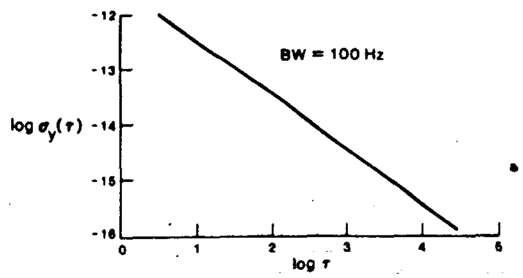

Fig. 5. Typical measurement noise floor.

approximately 1.5-ns phase uncertainty. To maintain 4-ps accuracy requires measurements simultaneous to 0.1 s.

8) There are no phase errors due to the switching of RF signals since there is no switching anywhere in the analog measurement system.

9) No appreciable phase errors are introduced when it is necessary to change the reference clock since, as shown in Fig. 4, the peak error due to changes in synthesizer phase is 20 ps.

10) The measurement system is capable of measuring its own phase noise when the same signal is applied to two input ports. Fig. 5 is the typical measured Allan variance plot. Error limits are not shown since unit-to-unit variations exceed the inaccuracy of the measurement. Long-term phase deviations were less than 25 ps peak to peak over a 40-day measurement period [4].

11) Since the IEEE-583 (CAMAC) interface standard has been followed for all the custom hardware, the system can be easily interfaced to almost any instrument controller. The system has already been tested using a large minicomputer, a small minicomputer, and a desk-top calculator. Interfaces between IEEE-583 and IEEE-488 controllers are available and have been used successfully.

12) The system is capable of comparing a very large number of oscillators at a reasonable cost per device.

Operating System

Design Considerations

Before discussing the operating system in detail, it is useful to outline exactly what we expect the system to do. We have identified the following general tasks that we expect the system to be able to perform: The programs must allow a variable number of clocks to be in the measurement ensemble at any time: the addition and deletion of clocks should be a simple matter that can be done by an operator with no special computer training. The programs must maintain an audit trail of changes to the ensemble of clocks being measured: this audit trail should be automatic and should not depend on the notebooks of the various users. The times of all of the clocks should be available for examination as soon after the data are recorded as is pratical. Any user should be able to examine the performance of any clock.

Although hardware failures are inevitable, the design should minimize the impact of a failure. The data-acquisition program is modular and each module is made as independent as possible. All input/output statements contain time-out loops so that a failure of any single clock module will not stop the program. All communication with the operator's console is done on a character-by-character basis under interrupt control, and these interrupts are ignored during a measurement cycle. Although the memory of the machine is volatile RAM, the state of the system is stored on disks, and the program can be stopped and restarted without any loss of data.

A final consideration is ease of use by people who are not computer experts. All commands and diagnostics are complete sentences (error numbers and computer jargon are not used). The parameters for all commands can be abbreviated for experienced users or spelled out in full for novices: the syntax for all commands is the same (verb or verb, noun or verb, noun, noun).

Hardware Limitations

In addition to incorporating the desirable features outlined above, the data-acquistion program had to recognize and cope with several limitations imposed by the hardware:

Each clock module contains two types of registers: a scaler that counts the number of zero crossings of the difference frequency between the clock being measured and the offset reference and a time-interval counter that measures the time interval between the zero crossings of the beat frequencies of the clock being measured and the reference each time a measurement is initiated. Note that the scaler advances continously while the time-interval counter only runs when a measurement is initiated. Both of these counters are 24 bits wide so that the maximum count is 16777215. If the difference frequency between any clock and the reference clock is 10 Hz, the epoch counter will overflow about every 19 days and some provision must be incorporated for detecting and removing these overflows (because of a peculiarity of the design, the counter, in fact, overflows after 8388607 counts or about every 9 days).

The scaler in each of the clock modules cannot be read without initiating a measurement cycle. The start measurement pulse is generated asynchronously by the minicomputer. It initiates a synchronization cycle which takes several cycles of the 10-Hz clock. Under worst case conditions, measurements can therefore only be made every 0.3 s. Thus the completion of a measurement cycle to read the elapsed time as indicated by the counter in the reference channel may be as much as two ticks late. Either some means must be provided of keeping time within the minicomputer or we must store the actual time of each reading and deal in all of the subsequent analysis with the fact that the intervals between the readings may not be exactly constant. We have chosen the former arrangement. The frequency of the reference clock is used to drive a software clock in the minicomputer. This clock maintains the time in conventional civil format including leap years. A real-time display shows the current software time, and the software tick may be synchronized to an external tick by a command from the operator's keyboard. The insertion of a leap second is also possible using a keyboard command.

Although each CAMAC crate can physically hold 11 clock modules, the pulse distribution system can only drive 6 modules. Thus each crate can only record the data from 24 clocks (4 clocks per module). The CAMAC system associates a unique electrical address with each physical slot in the crate (i.e., it is not a bus structure), and the program must map logical clock numbers to physical slots. This mapping must extend to multiple crate configurations, since 24 channels are unlikely to be sufficient for all applications.

Data Storage

The data storage scheme can record the data from up to 128 channels. Any channel may be active at any time; the active channels need not be contiguous.

The scheme is divided into three parts:

1) *The index file:* This file has one entry for each reading of the hardware. This entry is always of a fixed length and contains the time of the reading and the map of the active channels. It also contains various diagnostic information and a pointer to the start of the data in the data file.

2) *The data file:* This file has one entry for each reading of each clock. The readings for each time are grouped together in an area pointed to by the index file entry for that time. Since the number of active clocks may change, these entries are variable in length: the entries simply follow each other with no gaps. (The index file and the data file are logically related in the same way as the table of contents of a book is related to the text.)

3) *The identifier file:* This file has 128 entries—one for each potentially active channel. Each entry is a fixed length and contains the identities of the clocks connected to that channel in inverse chronological order (i.e., the current occupant is first and the oldest occupant is last). Each time the identity of a clock connected to a port is changed, that fact is recorded in the appropriate entry in this file by "pushing" the new entry onto a logical last-in-first-out stack. Thus the time history of each port is recorded. The programs will allow a clock to be connected only if the operator enters the serial number of the clock. This file may be accessed by any user to determine the identity of any clock in the ensemble. It is also used to annotate various outputs with the physical names of the clocks.

These files are maintained in two places: on a floppy disk connected to the minicomputer that reads the data and on a hard disk that is connected to the larger minicomputer that is used to analyze the performance of the clocks. The data are transmitted between these two files after every data-acquistion cycle using a serial data link between the two machines. The transmission protocol is a series of variable-length transmissions depending on how many clocks are active. The protocol contains full time-out protection and no data are lost if the larger minicomputer fails either during a transmission or any other time. The data are transmitted in a modified binary system and without loss of significance.

The floppy disk on the data-acquisition machine can store approximately 700 data scans: this is approximately two months worth of data at a sample rate of 12 times per day. This storage is totally independent of the larger minicomputer. If the larger computer is not working, the data-acquisition machine continues to accumulate data (and audit information if clocks are added or dropped). When the larger machine is operational again, all of the data since the last successful transmission are sent. This is accomplished automatically by the transmission protocol and requires no user intervention.

Data Retrieval and Analysis

The data may be examined by any user. Two types of access are provided: a group of utility tasks to provide the most commonly used functions such as plotting and listing and a group of library subroutines that may be incorporated into any user program. The library subroutines can be used to examine the data either sequentially in time or randomly. These routines allow full shared access among any number of users. All of the users access the files in read-only mode, and nonprivileged users cannot modify the data in any way. The data files are protected against unauthorized modification by the operating system and users need not concern themselves with the maintenance of the integrity of the data.

CONCLUSIONS

We have demonstrated a new phase measurement system with very desirable properties: All oscillators in the range of 5 MHz ± 5 Hz may be measured directly. The sampling times are only restricted by the requirement that they exceed one second. The noise floor is $\sigma_y(2, \tau) = 3 \times 10^{-12}/\tau$ in short term and the time deviations appear less than 25 ps in long term. All circuitry is designed as modules which allows expansion at modest cost. Compatibility with a variety of computers is insured through the use of the IEEE-583 interface and adapters are available to permit use with an IEEE-488 controller. The system makes it feasible to make completely automated phase measurements at predetermined times on large numbers of atomic clocks. It's own noise is one-hundred times less than the state of the art in atomic clock performance. The data may be accessed without interrupting the data-acquisition process and may be analyzed and plotted without danger of interferring with data collection or storage. The system is being used to make the measurements needed to compute NBS atomic time. It will also be very valuable for any laboratory which uses three or more atomic clocks.

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